ECE 272 Lab #4

Counters

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1. Introduction

This lab uses D-Flip-Flops to create a register used to store data. The objective is to design and implement a system on the FPGA using D-Flip-Flops to build a register with clock and reset buttons, Full Adders to build a Ripple-Carry Adder, and a decoder. This lab relies on piecing together the successful work of past labs. The software used is Quartus Prime 18 and ModelSim. The hardware used is a DE10-Lite FPGA, a USB-B cable, and my computer.

2. Design

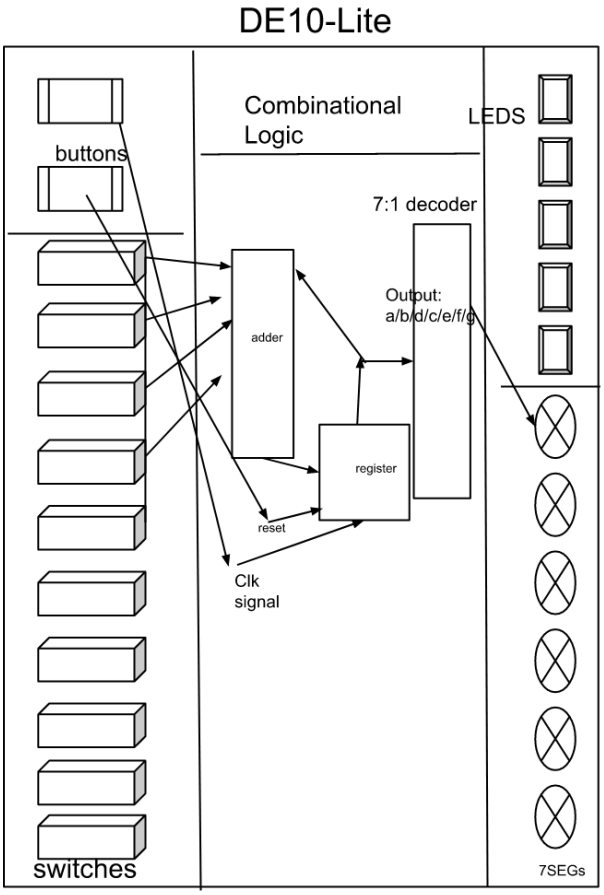

Figure 1: Combinational Logic

This depicts the combinational logic that will be used to complete the final schematic. It shows a ripple-carry adder, a register, a 7:1 decoder, and their inputs and outputs.

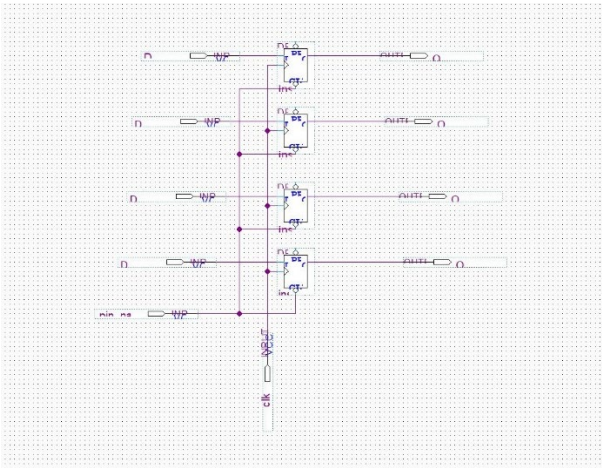

Figure 2: Register Schematic

This is one of the three modules that will be incorporated in the final design. This register is constructed from four D-flip-flops, and also has inputs connected to the clock and reset (CLRN) pins.

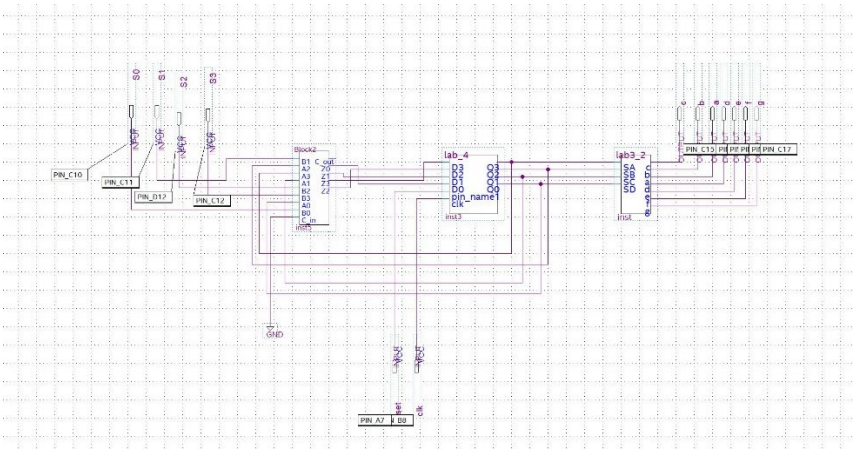

Figure 3: Total Counter Schematic

This displays the completed final schematic. It shows the switches leading to the counter, which has inputs and outputs connected to the register, whose final outputs lead to the 7:1 decoder.

Interface Name	Interface Purpose	Input or Output	Number of Pins	Active High or Low	Board Label	FPGA Pin
A	Gate Output	Output	1	LOW	7SEG00	C14
B	Gate Output	Output	1	LOW	7SEG01	E15
C	Gate Output	Output	1	LOW	7SEG02	C15
D	Gate Output	Output	1	LOW	7SEG03	C16
E	Gate Output	Output	1	LOW	7SEG04	E16
F	Gate Output	Output	1	LOW	7SEG05	D17
G	Gate Output	Output	1	LOW	7SEG06	C17
S0	Gate Input	Output	1	HIGH	Switch 0	C10
S1	Gate Input	Output	1	HIGH	Switch 1	C11
S2	Gate Input	Output	1	HIGH	Switch 2	D12
S3	Gate Input	Output	1	HIGH	Switch 3	C12
CLK	Gate Input	Output	1	LOW	Button 0	B8
RESET	Gate Input	Output	1	LOW	Button 1	A7

Figure 4: Design Interface

This figure depicts all the input and output pins as well as where they are mapped on the board.

3. Results

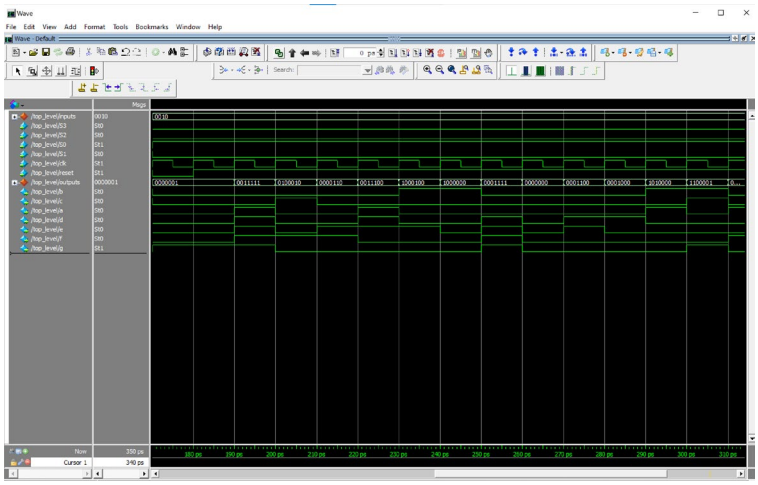

Figure 5: ModelSim Output 1

This figure shows the first portion of the ModelSim output, in which the seven segment display (outputs: a, b, c, d, e, f, g) are shown to be counting up by one based on the clock signal and input switch.

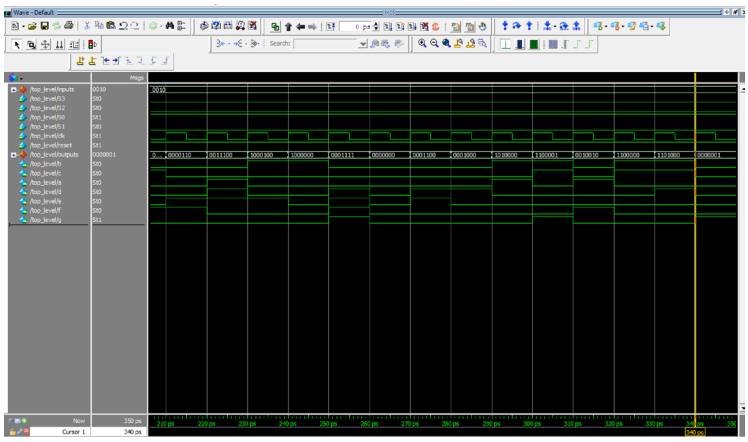

Figure: ModelSim Output 2

This is the rest of the ModelSim output showing the counter operating effectively.

4. Experiment Notes

The lab was straightforward, so I thought I would have an easy time with it. I was sorely mistaken. I spent many hours troubleshooting my input-output connections only to realize I did not know which inputs were what, as I could not see the full label. I just assumed Quartus would put them in order, and again I was mistaken. My display was having compatibility issues with Quartus leading to the blocks not displaying their full input/output labels. After I fixed this, I was able to resolve all other issues in less than thirty minutes. I learned to never place my trust in software.

5. Study Questions

1. There are several different types of counters, one of which we designed. Other counters include a synchronous counter and decade counter. In a decade counter, a NAND gate is connected to several D-flip-flops. In a synchronous counter, two AND gates are wired to several flip flops, all of which have one global clock.

Source: https://www.geeksforgeeks.org/counters-in-digital-logic/

2. PRN stands for presetnot, and CLRN stands for clearnot. They are both active low. Preset sets Q, and clear clears it. CLRN and PRN are both asynchronous. The “N” stands for not, and is what indicates that they are active low. CLRN sets Q to 0, while PRN sets Q to 1.

3. In my lab, I connected a wire to all CLRN ports of the four D-flip-flops, which was then connected to a push button, which was also active low. This implemented a reset function where the value of Q was cleared and returned to 0 so the counting could begin again.